REMARKS

A telephone interview between Examiner Schwartz and Dennis Smid (one of the applicant's undersigned attorneys) was held on December 22, 2009. The applicant and Mr. Smid wish to thank the Examiner for his time and consideration for such discussion.

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over JP 02249333 (Hirade, Junji et al.), in view of U.S. Patent No. 4,71,3605 A (Iyer et al.).

As discussed during the December 22 discussion and as previously indicated, claims 1-7 have been canceled herein. Such cancellation should not be construed as an indication that the applicant agrees with the above 103 rejection. Applicant reserves the right to file one or more continuation applications directed to any one or ones of the canceled claims.

Claims 10-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,535,239 A (Padovani et al.), in view of U.S. Patent No. 4,827,514 A (Ziolko et al.), in further view of U.S. Patent No. 3,784,783 A (Schroeder).

Independent claims 10 and 15 have been amended herein in the manner discussed during the December 22 discussion. As a result and as an example, amended independent claim 10 now recites in part the following:

> "a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift register, and a first adder, said random number generating circuit being arranged such that (i) **an output stage of the first shift register is directly coupled to**

> **an input stage of the second shift register and to the first adder such that during operation an output from the first shift register is supplied to the input stage of the second shift register and the same output from the first shift register is supplied to an input of the first adder**, and (ii) **an output stage of the second shift register is directly coupled to the first adder such that during operation an output of the second shift register is supplied to another input of the first adder**;
>
> . . .
>
> a first switch arranged to receive the scramble-processed data **from the second adder** and the bit data of the predetermined pattern from the data generator, said first switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the scramble-processed data when synchronization processing of the transmit data is not performed and to output the data selected." (Emphasis added.)

It is respectfully submitted that the present application provides support for the features herein added to claim 10 (and to claim 15). With regard thereto and as an example, reference is made to lines 1-6 of page 12 and Fig. 4, along with Figs. 6 and 8 and the corresponding portions of the present application.

In explaining the above 103 rejection, the Examiner stated that the "combination of Padovani and Ziolko do not expressly disclose that during operation an output from the first shift register is supplied to the input stage of the second shift register and to an input of the first adder and during operation an output of the second shift register is supplied to another input of the first added." (See line 20 of page 9 to line 2 of page 10 of the present Office Action.) The Examiner then stated that Schroeder (and in particular elements

23, 25, 27, and 30 of Fig. 1 and lines 20-21, 28-31, and 58-65 of column 3 thereof) teaches such features. (See lines 3-7 of page 10 of the present Office Action.)

As discussed during the December 22 discussion, it is respectfully submitted that the portions of Schroeder relied on by the Examiner do not appear to disclose "(i) . . . such that during operation an output from the first shift register is supplied to the input stage of the second shift register and the same output from the first shift register is supplied to an input of the first adder, and (ii) . . . such that during operation an output of the second shift register is supplied to another input of the first adder" as now recited in claim 15.

As also discussed during the December 22 discussion, it is somewhat unclear what reference and which element therein the Examiner is relying on for the second adder of claim 10. As such, and as also discussed during the December 22 discussion, it is respectfully submitted that Ziolko as applied by the Examiner does not appear to a first switch "arranged to receive the scramble-processed data from the second adder and the bit data of the predetermined pattern from the data generator" as in claim 10.

Accordingly, for at least the above-described reasons, it is respectfully submitted that amended claim 10 is distinguishable from the combination of Padovani, Ziolko, and Schroeder.

For at least some of the reasons previously described with regard to claim 10 or reasons similar thereto, it is also respectfully submitted that amended independent claim 15 is also distinguishable from the applied combination of Padovani, Ziolko, and Schroeder.

Claims 11-14 are dependent from amended independent claim 10. Accordingly, it is also respectfully submitted that dependent claims 11-14 are distinguishable from the applied

combination of Padovani, Ziolko, and Schroeder for at least the reasons previously described.

As it is believed that all of the rejections set forth in the Official Action have been overcome, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional rejections and/or objections which the Examiner might have.

If there are any charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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